ABSTRACT

In one disclosed embodiment an instruction loop having at least one instruction is identified. For example, each instruction can be a VLIW packet comprised of several individual instructions. The instructions of the instruction loop are fetched from a program memory. The instructions are then stored in a register queue. For example, the register queue can be implemented with a head pointer which is adjusted to select a register in which to write each instruction that is fetched. It is then determined whether the processor requires execution of the instruction loop, for example, by checking a program counter (PC) value corresponding to each instruction. When the processor requires execution of the instruction loop, the instructions are output from the register queue. For example, the register queue can be implemented with an access pointer which is adjusted to select a register from which to output each instruction that is required.